IN THE SPECIFICATION:

Please amend the specification as follows:

Please substitute the following paragraphs for the same-numbered paragraphs in the specification:

[0011] In order to attain the objects suggested above, there is provided, according to one aspect of the invention, a comparator comprising at least two transistor, wherein the comparator is ~~a circuit for setting~~ set to have a first trip point corresponding to ~~of~~ a rising edge of an input signal according to a value of an external voltage reference, and ~~at least two transistors in the circuit for setting the~~ a second trip point corresponding to ~~of~~ a falling edge of the input signal according to the width to length ratio of the at least two transistors.

[0043] This outset condition is shown in the graphical HSPICE circuit simulation results of FIG. 7 at time 0 ~~1/4~~ µs. FIG. 7 shows three wave forms, including the external reference voltage V_{REF}, which maintains a fixed voltage of 600 mV throughout the simulation depicted by the wave form having the triangle symbol at its left edge. The COMPIN signal, indicated by the circle symbol on the left edge of its wave form, is a periodic triangularly shaped wave form varying in amplitude between 0 V and 2.2 V with a period of approximately 31 ~~1/4~~ µs. The COMPOUT signal, shown by the wave form indicated with an X symbol at the left edge of the wave form, varies between 0 V and 1.8 V in amplitude. At time 0 ~~1/4~~ µs, V_{REF} is 600 mV, COMPIN is 0 V, and COMPOUT is 1.8 V.

[0045] This situation is shown in the HSPICE circuit simulation results of FIG. 7 at time 5 ~~1/4~~ µs, where the rising COMPIN voltage crosses the trip point voltage of 600 mV set by V_{REF}. This causes the COMPOUT voltage to fall to 0 V. In this state, the seven transmission gates of FIG. 1 and FIG. 2 change their state since the control voltages at nodes n1 and n2 have changed their polarity. Thus, transmission gates, which were previously opened, are now closed and vice-versa.

[0047] As the COMPIN voltage begins to fall, indicated at a time of approximately 16 ~~1/4~~ µs in FIG. 7, the trip/point becomes dependent on the width-to-length ratio $(W_{T1}/L_{T1})/(W_{T3}/L_{T3})$ which is equivalent to $(W_{T1}/L_{T1})(L_{T3}/W_{T3})$ for transistors T1 and T3. In the Schmitt trigger of FIG. 6, transistor T2 is the main switching device, while T1 and T3 act as a feedback network that controls the falling edge trip point. By adjusting the aspect ratio of these two transistors, the falling edge trip point V- can be controlled. For a Schmitt trigger, V- is defined in the literature in equation form as:

$$V^- = [SQRT\{(W_{T1}/L_{T1})(L_{T3}/W_{T3})\}\{V_{CC}-V_{tp}\}] / [1+SQRT\{(W_{T1}/L_{T1})(L_{T3}/W_{T3})\}] \quad \text{Equation 1}$$

[0050] As the COMPIN voltage continues to fall between times 16 ~~1/4~~ µs and 31 ~~1/4~~ µs in FIG. 7, it crosses the V_{REF} voltage of 600 mV with no change occurring in COMPOUT. Continuing the voltage descent, COMPIN passes through the 110 mV mark at a time of approximately 30 ~~1/4~~ µs which results in COMPOUT transitioning from 0 V to 1.8 V. This indicates that the inventive comparator has transformed itself back into the analog configuration,

which was evident at the outset because COMPIN falls below the trip point established by the aspect ratios of transistors T1 and T3.

[0051] Furthermore, the transmission gate control nodes n1 and n2 also change polarity and return to the initial value they held at time 0 ~~ì¼s~~ µs in FIG. 7. FIG. 7 shows two comparison cycles with each cycle approximately 31 ~~ì¼s~~ µs in duration. In the first comparison cycle between times 0 ~~ì¼s~~ µs and 31 ~~ì¼s~~ µs, the inventive comparator is in the analog configuration between time 0 ~~ì¼s~~ µs to 5 ~~ì¼s~~ µs and time 30 ~~ì¼s~~ µs to 31 ~~ì¼s~~ µs for a total of 6 ~~ì¼s~~ µs, and in the digital configuration between time 5 ~~ì¼s~~ µs and 30 ~~ì¼s~~ µs for a total of 25 ~~ì¼s~~ µs. This clearly shows that the comparator is in the power saving digital mode for more than 80% of the comparison cycle time.

[0052] FIG. 8 shows the results of an HSPICE circuit simulation illustrating the power saving feature of the inventive comparator. The COMPIN and V_{REF} waveforms indicated with the X and circle symbols, respectively, are identical to those as seen in FIG. 7. The additional waveform in FIG. 8, indicated by the square symbol at the left edge of the waveform, is the current through the VCC positive power supply. At time 2.11 ~~ì¼s~~ µs and also at time 32.5 ~~ì¼s~~ µs, when the comparator is in the analog configuration, the current through V_{CC} is 3.19 ~~ì¼A~~ µA. At time 16.4 ~~ì¼s~~ µs and also at time 47.8 ~~ì¼s~~ µs, when the comparator is in the digital configuration, the current through V_{CC} is only 13.8 nA.

[0053] The data in Table 1 demonstrates that a wide voltage range is achievable for the falling edge trip point voltage V^-. Additionally, when adjusting the transistor aspect ratios of T1 and T3, it is preferable to only adjust the aspect ratio of T1 because T2 and T3 should be identical for the case, where COMPIN is rising and the comparator is in the analog configuration described previously. Any limitations on the width-to-length ratios of T1 and T3 are due to the minimum manufacturable transistor channel width and length allowed by the particular CMOS technology. In general, however, the ratio (W_{T1} / L_{T1}) will be much less than 1 and the ratio (W_{T3} / L_{T3}) will be much greater than 1. As an example, in a 0.18 ~~μm~~ μm technology, (W_{T1} / L_{T1}) might assume a value of 1 ~~μm~~ μm / 32 ~~μm~~ μm, resulting in a ratio of 0.03125, and (W_{T3} / L_{T3}) could be realized in a value of 48 ~~μm~~ μm / 0.18 ~~μm~~ μm for a ratio of 266.667, where L_{T3} is the minimum channel length.